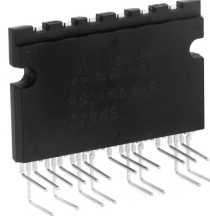
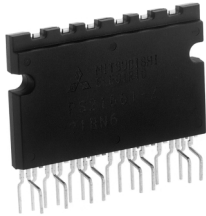


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INTEGRATED POWER FUNCTIONS

- 600V/3A low-loss 5th generation IGBT inverter bridge for 3 phase DC-to-AC power conversion.

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

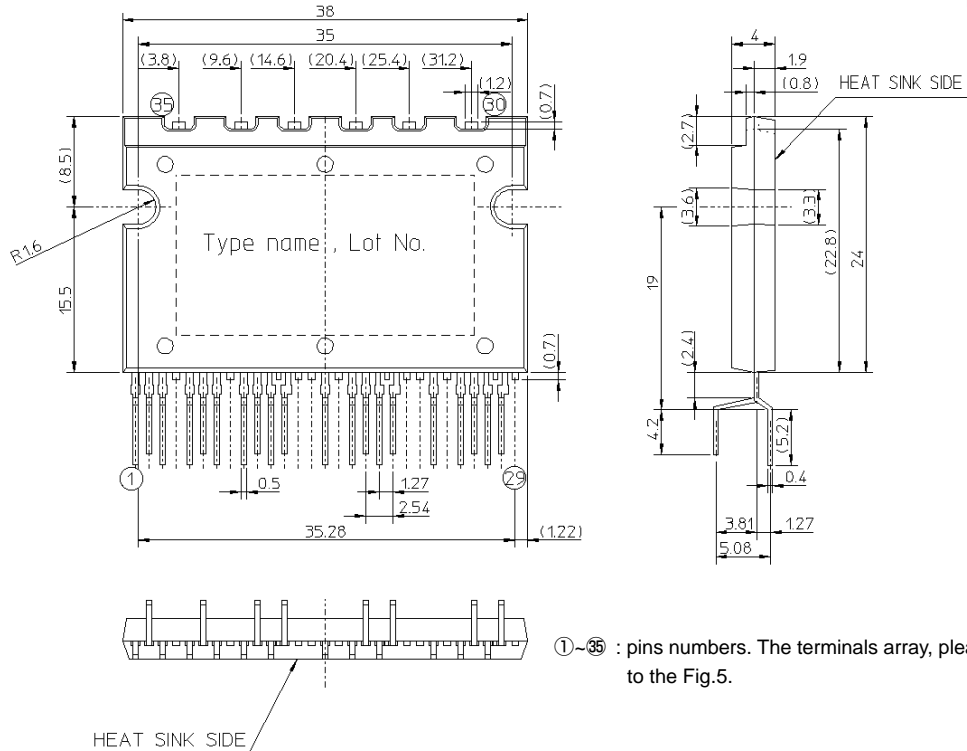
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage protection (UV).
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible Schmitt Trigger receiver circuit (Active high), Arm-short-through interlock protection.

APPLICATION

AC100V~200V, three-phase inverter drive for small power motor control.

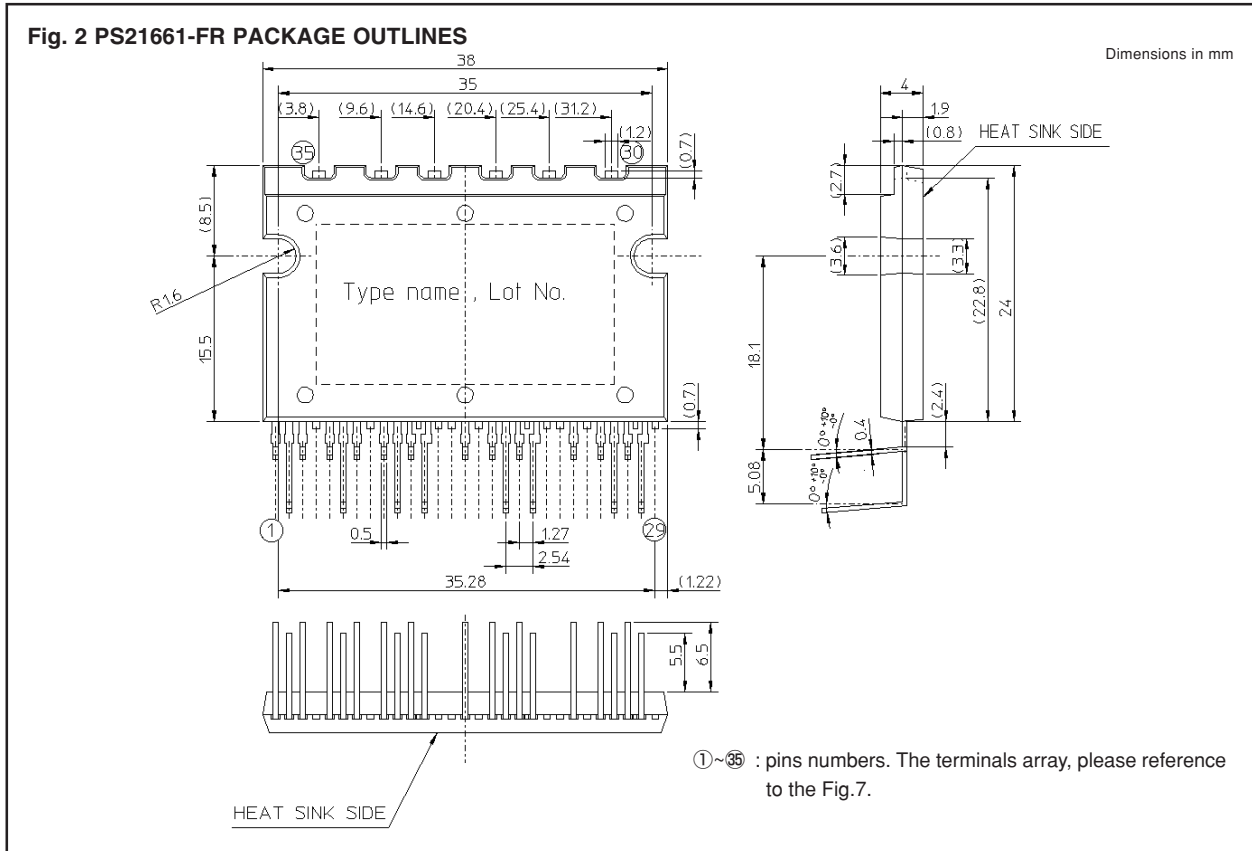
Fig. 1 PS21661-RZ PACKAGE OUTLINES

Dimensions in mm



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	500	V
VCEs	Collector-emitter voltage		600	V
$\pm I_C$	Collector current	$T_f = 25^\circ\text{C}$	3	A
$\pm I_{CP}$	Collector current (peak)	$T_f = 25^\circ\text{C}$, $t_w \leq 1\text{msec}$	6	A
Pc	Collector dissipation	$T_f = 25^\circ\text{C}$, per 1 chip	13.8	W
Tj	Junction temperature	(Note 1)	-20~+150	$^\circ\text{C}$

Note 1 : The maximum junction temperature rating of the power chips integrated within the SIP-IPM is 150°C ($@ T_f \leq 100^\circ\text{C}$) however, to insure safe operation of the SIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125^\circ\text{C}$ ($@ T_f \leq 100^\circ\text{C}$).

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-U (VUFS), VVFB-V (VVFS), VWFB-W (VWFS)	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP-VNC, UN, VN, WN-VNC	-0.5~V _D	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D	V
I _{FO}	Fault output current	Sink current at FO terminal	10	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D	V

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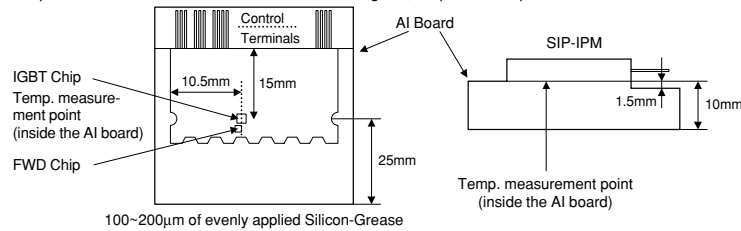
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TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Self protection supply voltage limit (short circuit protection capability)	VD = 13.5~16.5V, Inverter part Tj = 125°C start, non-repetitive, less than 2 μs	400	V
Tf	Heatsink operation temperature	(Note 2)	-20~+100	°C
Tstg	Storage temperature		-40~+125	°C
Viso	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	Vrms

Note 2 : Tf MEASUREMENT POINT

AI Board Specification : Dimensions 50 × 50 × 10mm, finishing 12s, warp -50~+100μm



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Rth(j-f)Q	Junction to fin thermal resistance	Inverter IGBT part (per 1/6 module) (Note 3)	—	—	9.0	°C/W
Rth(j-f)F		Inverter FWD part (per 1/6 module) (Note 3)	—	—	9.0	

Note 3 : Grease with good thermal conductivity should be applied evenly about +100μm ~ +200μm on the contact surface of SIP-IPM and a heat-sink.

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
VCE(sat)	Collector-emitter saturation voltage	VD = VDB = 15V VIN = 5V	—	1.60	2.15	V
		IC = 3A, Tj = 25°C IC = 3A, Tj = 125°C	—	1.70	2.30	
VEC	FWD forward voltage	Tj = 25°C, -IC = 3A, VIN = 0V	—	1.55	2.00	V
ton	Switching times	VCC = 300V, VD = 15V IC = 3A, Tj = 125°C Inductive load (upper-lower arm) VIN = 0 ↔ 5V	0.35	0.70	1.10	μs
tr			—	0.20	—	μs
tc(on)			—	0.35	0.55	μs
toff			—	1.00	1.50	μs
tc(off)			—	0.55	1.10	μs
ICES	Collector-emitter cut-off current	VCE = VCES	—	—	1	mA
		Tj = 25°C Tj = 125°C	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
Id	Circuit current	VD = 15V, VIN = 0V	—	—	3.60	mA	
		VD = 15V, VIN = 5V	—	—	3.90		
IDB		VDB = 15V, VIN = 0V	—	—	0.50	mA	
		VDB = 15V, VIN = 5V	—	—	0.50		
VFOH	Fault output voltage	VSC = 0V, FO circuit : 1kΩ to 5V pull-up	4.9	—	—	V	
VFOL		VSC = 1V, IFO = -10mA	—	—	0.95	V	
IIN	Input current	VIN = 5V	0.70	1.06	1.50	mA	
VSC(ref)	Short circuit trip level	Tj = 25°C, VD = 15V (Note 4)	0.43	0.48	0.53	V	
UVDBt	Supply circuit under-voltage protection	Tj ≤ 125°C	Trip level	10.0	—	12.0	V
UVDBr			Reset level	10.5	—	12.5	V
UVDt			Trip level	10.3	—	12.5	V
UVDr			Reset level	10.8	—	13.0	V
tFO	Fault output pulse width	(Note 4)	20	40	—	μs	
Vth(on)	ON threshold voltage	Applied between:	2.10	2.35	2.60	V	
Vth(off)	OFF threshold voltage	UP, VP, WP-VNC, UN, VN, WN-VNC	1.10	1.40	1.80	V	

Note 4 : Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 5.1A

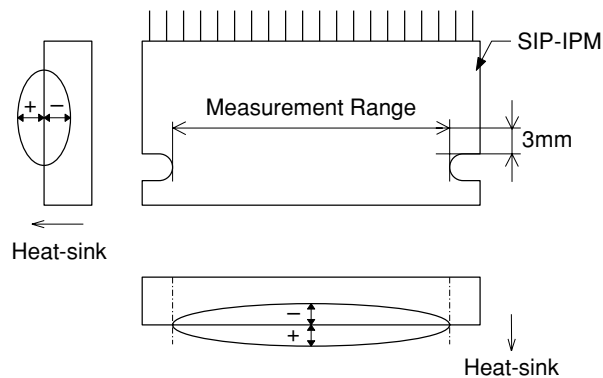
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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : (M3)	0.59	0.69	0.78	N·m
Weight		—	10	—	g
Heat-sink flatness	(Note 5)	-50	—	+100	μm

Note 5: Measurement point of heat-sink flatness



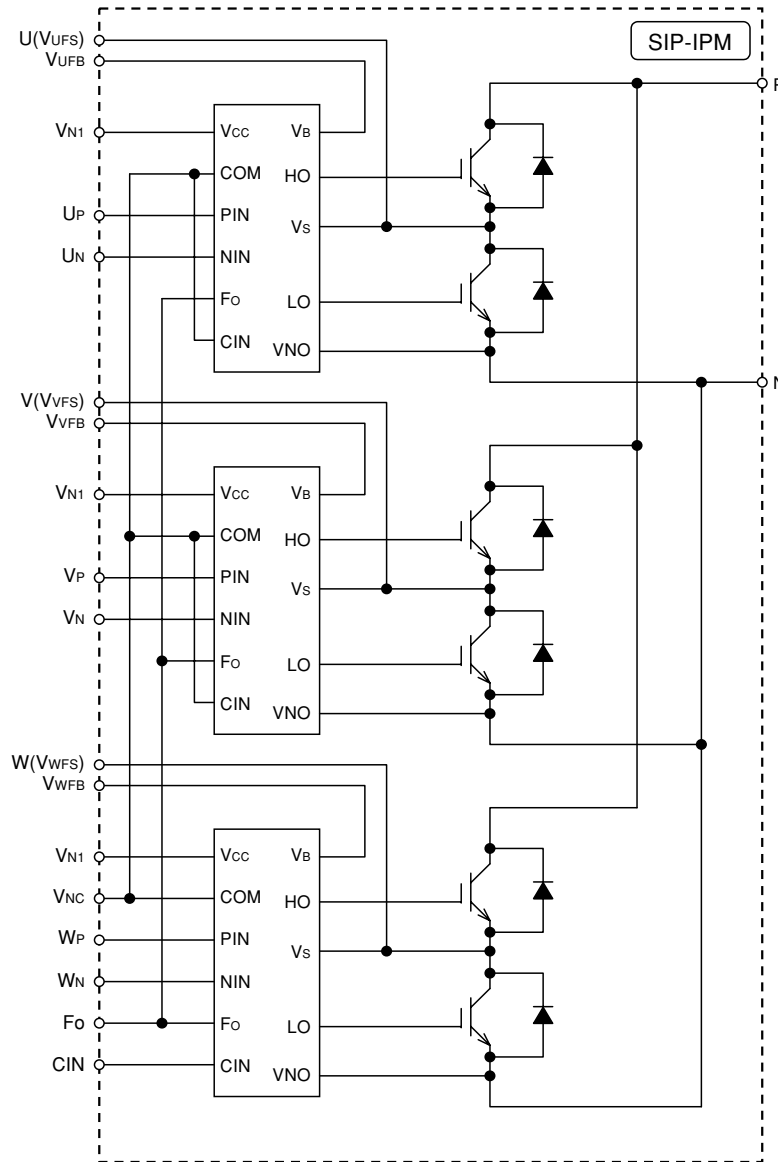
RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage	Applied between P-N	0	300	400	V
V _D	Control supply voltage	Applied between V _{N1} -V _{NC}	13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between V _{UFB-U} (V _{UFS}), V _{VFB-V} (V _{VFS}), V _{WFB-W} (V _{WFS})	13.0	15.0	18.5	V
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs
t _{dead}	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through	1.5	—	—	μs
f _{PWM}	PWM input frequency	T _j ≤ 125°C, T _f ≤ 100°C	—	15	—	kHz
I _O	Allowable r.m.s current	V _{CC} = 300V, V _D = 15V, f _C = 15kHz, P.F = 0.8, sinusoidal T _j ≤ 125°C, T _f ≤ 100°C	—	—	1.5	Arms
V _{NC}	V _{NC} terminal voltage	Applied between V _{NC} -N (include surge voltage)	-5	—	5	V
t _{XX}	minimum on pulse width	U _P , V _P , W _P , U _N , V _N , W _N terminal	0.7	—	—	μs

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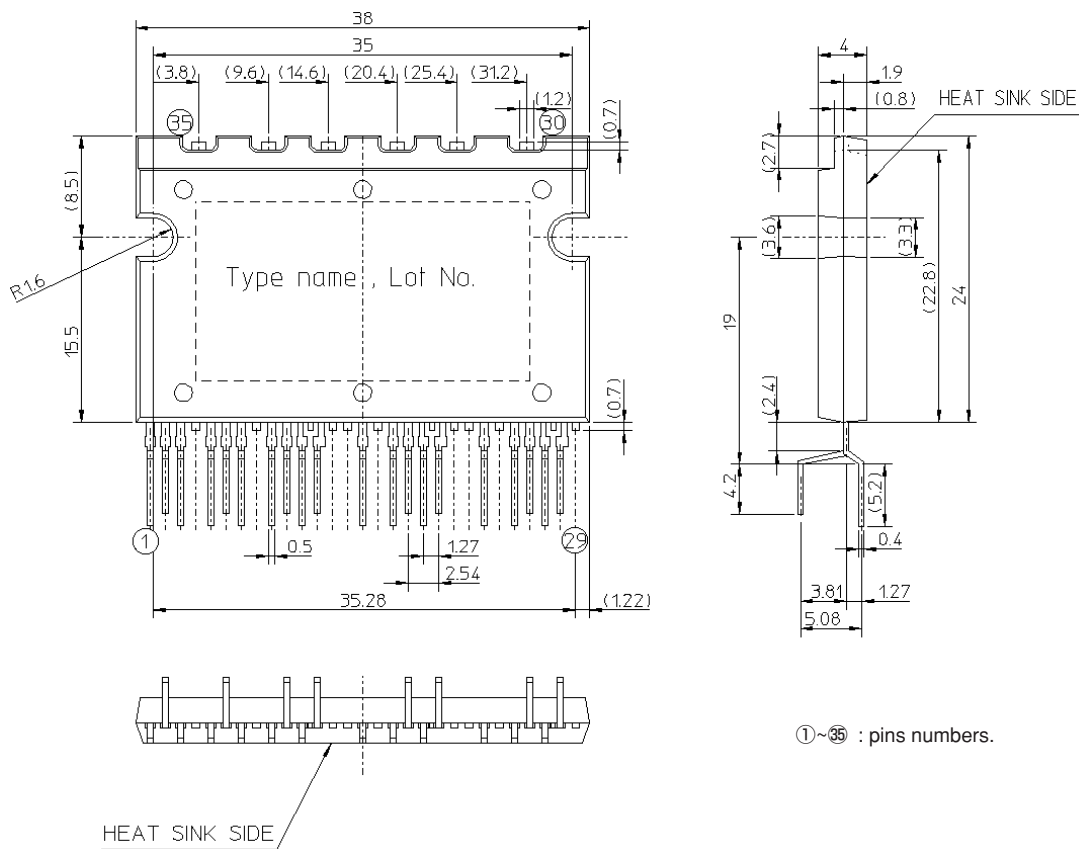
Fig. 3 THE SIP-IPM INTERNAL CIRCUIT



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Fig. 4 PS21661-RZ PACKAGE OUTLINES



①~③⑤ : pins numbers.

Terminal No	Symbol	Description
1	N	Inverter DC-link negative (GND) terminal
2	P	Inverter DC-link positive terminal
3	Fo	Fault output terminal
5	V _{NC}	Control GND terminal
6	CIN	Short-circuit trip voltage sensing terminal
7	V _{N1}	Control supply terminal
9	W _N	W-phase N-side control input terminal
10	V _{WFB}	W-phase P-side drive supply terminal
11	W _P	W-phase P-side control input terminal
12	W(V _{WFS})	W-phase inverter output terminal (W-phase P-side drive supply GND terminal)
15	V _{N1}	Control supply terminal
17	V _N	V-phase N-side control input terminal
18	V _{VFB}	V-phase P-side drive supply terminal
19	V _P	V-phase P-side control input terminal
20	V(V _{VFS})	V-phase inverter output terminal (V-phase P-side drive supply GND terminal)
23	V _{N1}	Control supply terminal
25	U _N	U-phase N-side control input terminal
26	V _{UFB}	U-phase P-side drive supply terminal
27	U _P	U-phase P-side control input terminal
28	U(V _{UFS})	U-phase inverter output terminal (U-phase P-side drive supply GND terminal)

The following pins are dummy pins are therefore should not be connected.
4,8,13,14,16,21,22,24,29,30~35 (30~35 are the high voltage side pins.)

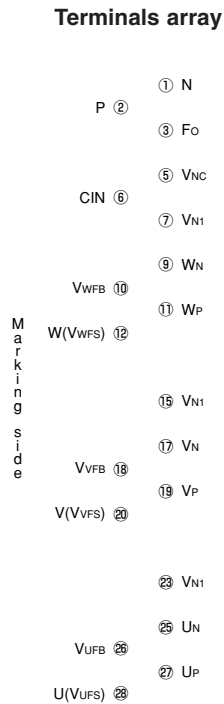
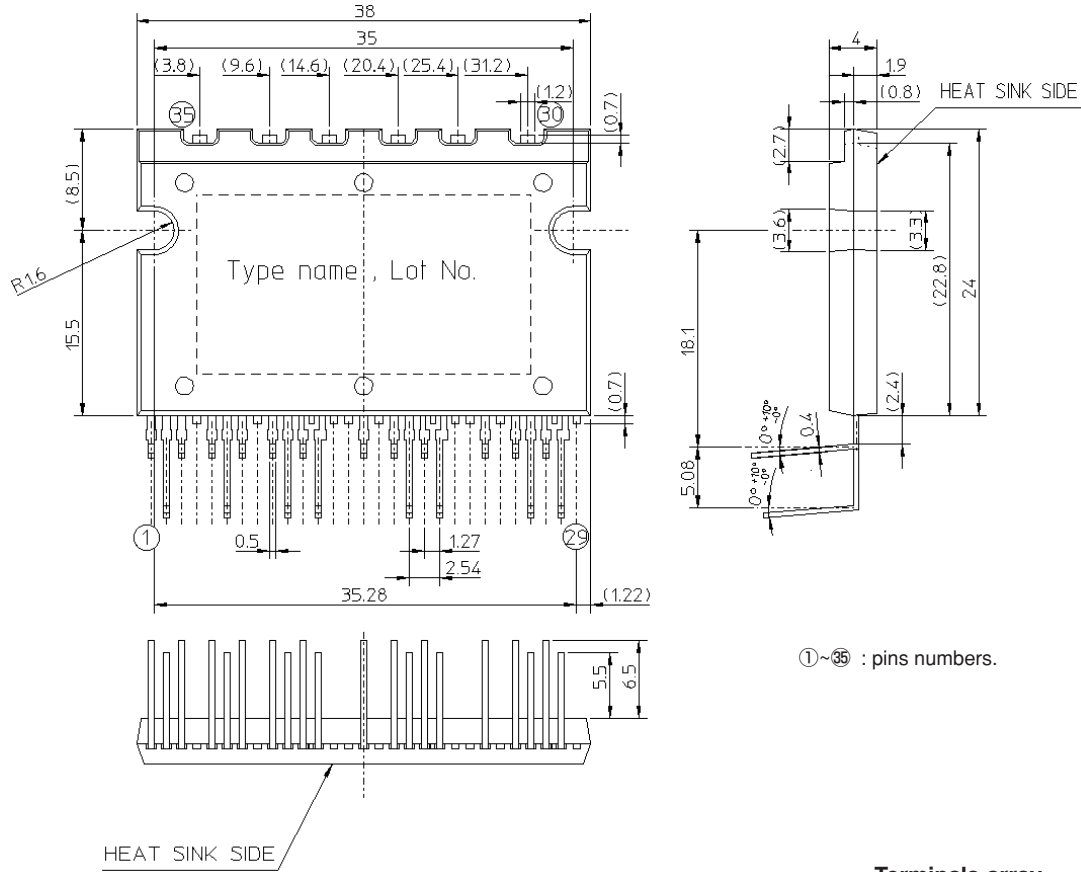


Fig. 5

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Fig. 6 PS21661-FR PACKAGE OUTLINES



①~③⑤ : pins numbers.

Terminal No	Symbol	Description
1	N	Inverter DC-link negative (GND) terminal
2	P	Inverter DC-link positive terminal
3	Fo	Fault output terminal
5	VNC	Control GND terminal
6	CIN	Short-circuit trip voltage sensing terminal
7	VN1	Control supply terminal
9	WN	W-phase N-side control input terminal
10	VWFB	W-phase P-side drive supply terminal
11	WP	W-phase P-side control input terminal
12	W(VWFS)	W-phase inverter output terminal (W-phase P-side drive supply GND terminal)
15	VN1	Control supply terminal
17	VN	V-phase N-side control input terminal
18	VVFB	V-phase P-side drive supply terminal
19	VP	V-phase P-side control input terminal
20	V(VVFS)	V-phase inverter output terminal (V-phase P-side drive supply GND terminal)
23	VN1	Control supply terminal
25	UN	U-phase N-side control input terminal
26	VUFB	U-phase P-side drive supply terminal
27	UP	U-phase P-side control input terminal
28	U(VUFS)	U-phase inverter output terminal (U-phase P-side drive supply GND terminal)

The following pins are dummy pins and therefore should not be connected.
4,8,13,14,16,21,22,24,29,30~35 (30~35 are the high voltage side pins.)

Terminals array

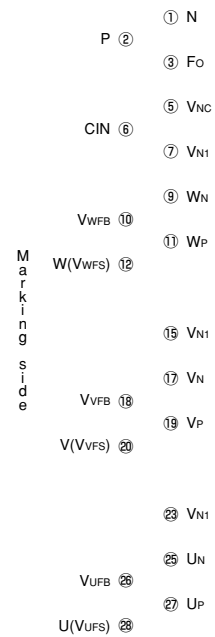
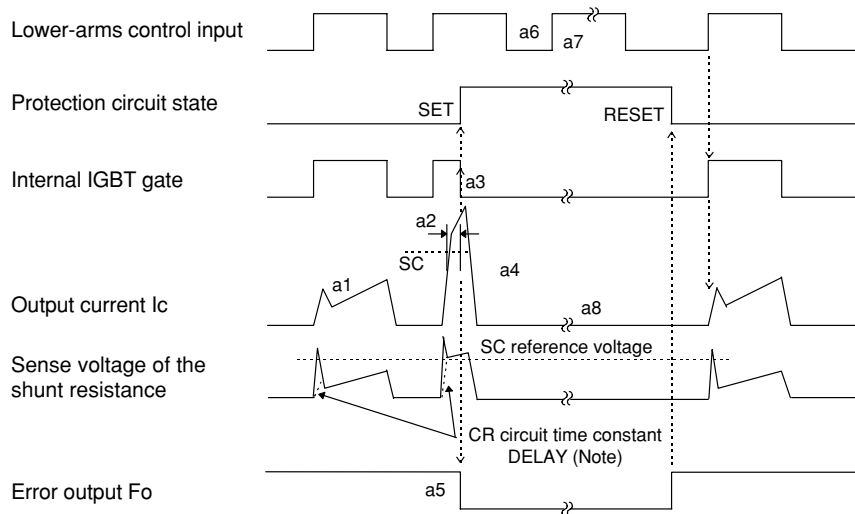


Fig. 7

Fig. 8 TIMING CHARTS OF THE SIP-IPM PROTECTIVE FUNCTIONS

[A] Short-Circuit Protection (Lower-arms only)

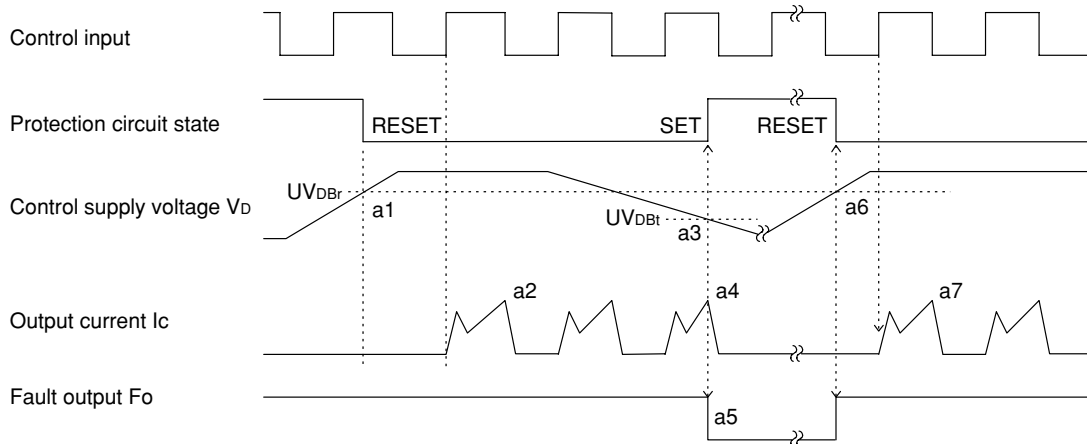
- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. Hard IGBT gate interrupt.
- a4. IGBT turns OFF.
- a5. Fo output (20~80μs).
- a6. Input "L" : IGBT OFF state.
- a7. Input "H" : IGBT ON state, but during the Fo active signal the IGBT doesn't turn ON.
- a8. IGBT OFF state.



Note : The CR time constant safe guards against erroneous SC signal resulting from di/dt generated voltages when IGBT turns ON. The optimum setting for the CR circuit time constant is 1.5~2.0μs.

[B] Under-Voltage Protection (Lower-arms, UVd)

- a1. Control supply voltage rises : After the voltage level reaches UVDr, the circuits start to operate when the next input is applied.
- a2. Normal operation : IGBT ON and carrying current.
- a3. Under voltage trip (UVdt).
- a4. IGBT OFF in spite of control input condition.
- a5. Fo output (20~80μs).
- a6. Under voltage reset (UVDr).
- a7. Normal operation : IGBT ON and carrying current.

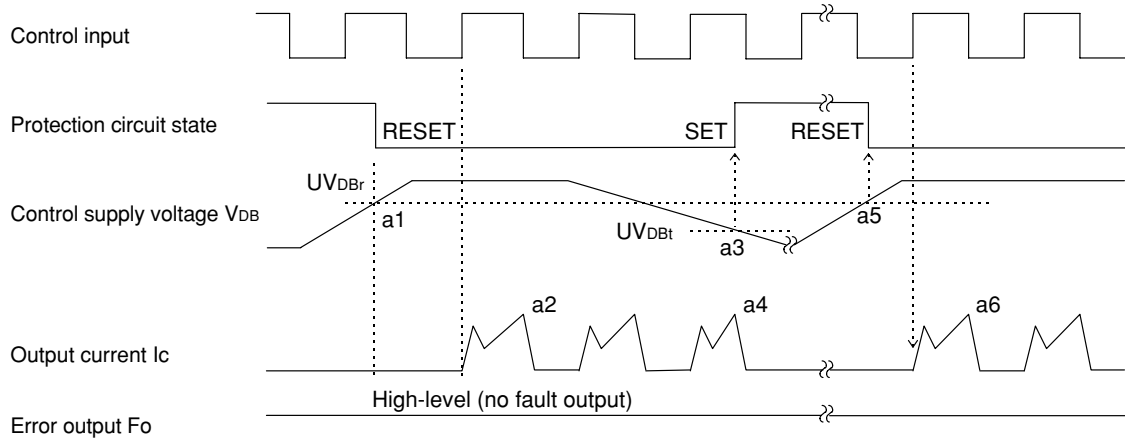


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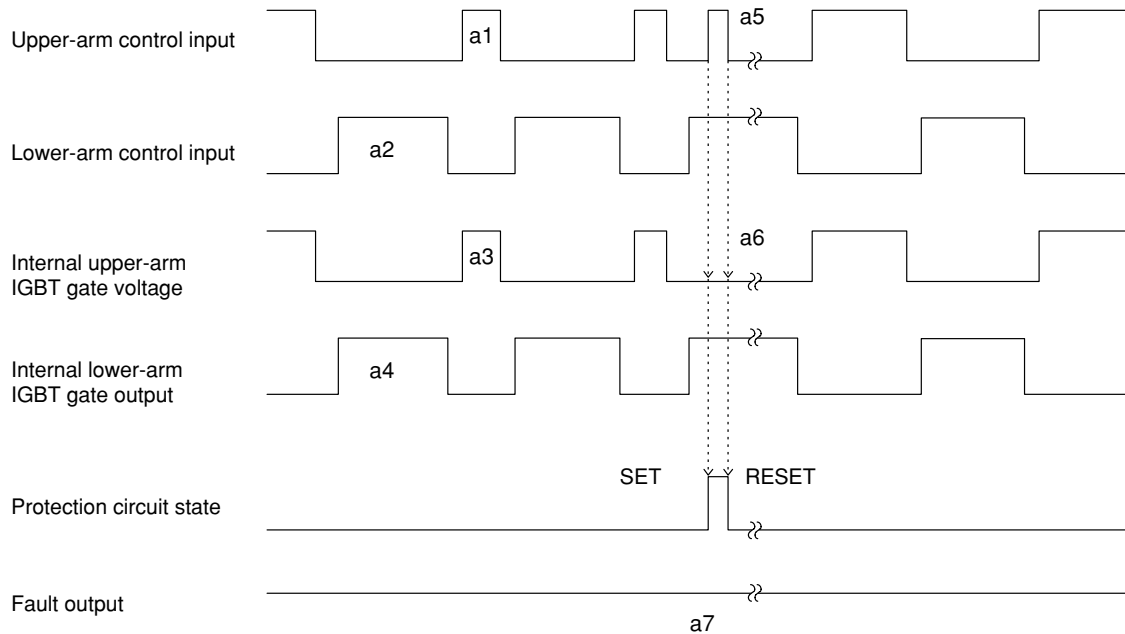
[C] Under-Voltage Protection (Upper-arms, UVDB)

- a1. Control supply voltage rises : After the voltage level reaches UVDBr, the circuits start to operate when the next input is applied.
- a2. Normal operation : IGBT ON and carrying current.
- a3. Under voltage trip (UVDBt).
- a4. IGBT OFF in spite of control input condition, but there is no Fo signal output.
- a5. Under voltage reset (UVDBr).
- a6. Normal operation : IGBT ON and carrying current.



[D] Simultaneous input signal prevention function

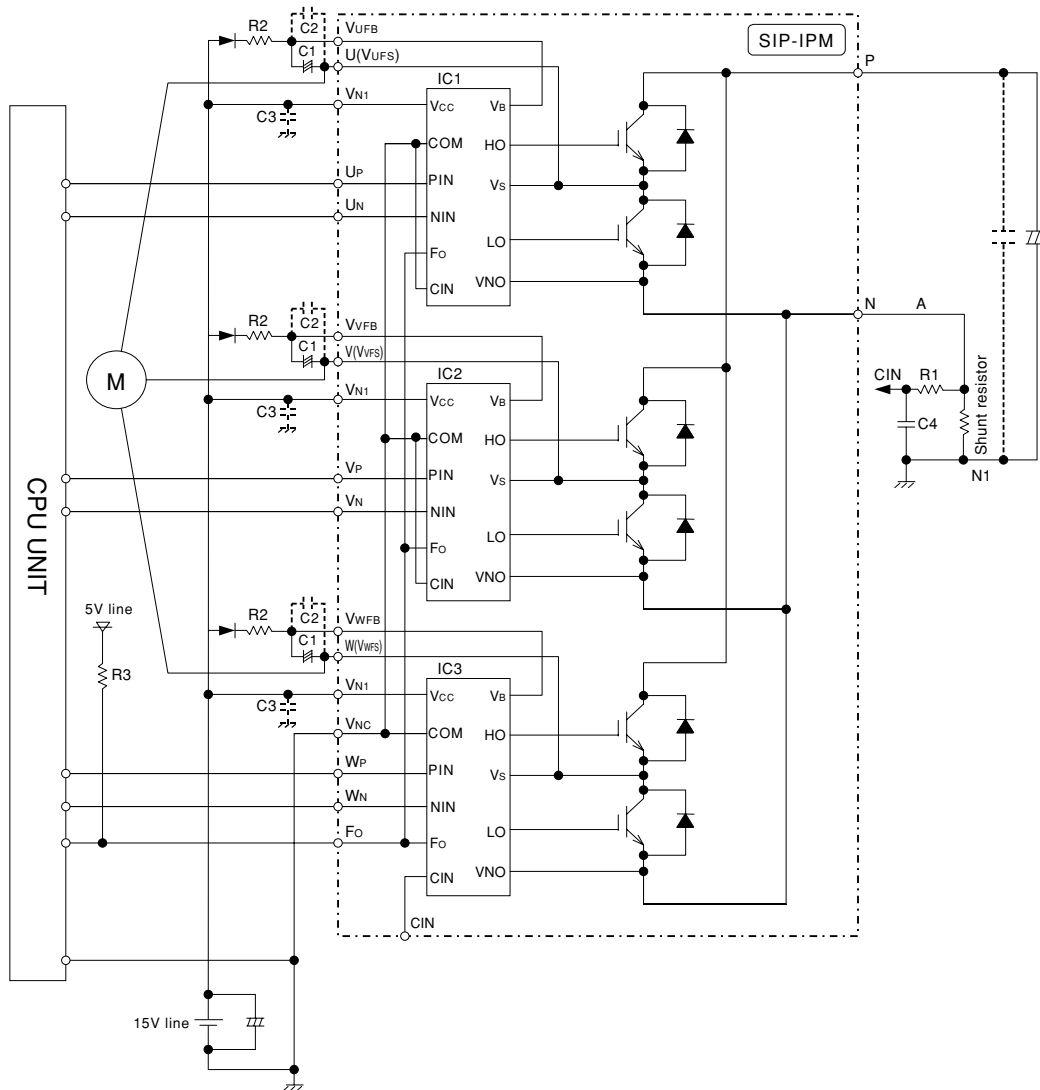
- a1 a3. Normal operation : IGBT ON and outputting IGBT gate voltage.
- a2 a4. Normal operation : IGBT ON and outputting IGBT gate voltage.
- a5. Abnormal pulse input.
- a6. IGBT OFF state.
- a7. No fault output.



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Fig. 9 TYPICAL SIP-IPM APPLICATION CIRCUIT EXAMPLE



Note 1 : Input signal lines are pulled-down with 4.7kΩ (min.) internal resistor. If these input lines are susceptible to noise, an RC coupling at each input is recommended. Input signal voltage is determined by the values of internal pull-down resistor and the external connected resistor. Set the external resistance value so that input signal voltage exceeds the on-threshold voltage. To prevent the input signals oscillation, the wiring of each input should be as short as possible.

2 : By virtue of integrating the specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3 : Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 1kΩ resistance.

4 : Approximately a 0.1~2μF by-pass capacitor should be used across each power supply connection terminals.

5 : To prevent errors of the protection function, the wiring of A should be as short as possible.

6 : Each capacitor should be located as close to the pins of the SIP-IPM as possible.

7 : In the recommended protection circuit, please select the R1C4 time constant in the range of 1.5~2μs.

8 : To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P&N1 pins is recommended.